

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		10550326
	Filing Date		2005-09-23
	First Named Inventor	Roger D. Chamberlain	
	Art Unit	2439	
	Examiner Name	Tolentino, Roderick	
Attorney Docket Number		53047-57365	

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	5	6625150		2003-09-23	Yu		
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9	7496108		2009-02-24	Biran et al.	
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	4	20040111632		2004-06-10	Halperin	
	5	20050135608		2005-06-23	Zheng	

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6	20050229254		2005-10-13	Singh et al.	
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	5	2000286715	JP	A	2000-10-13	Toshiba Corp		<input type="checkbox"/>
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	2	ASAMI ET AL., "Improvement of DES Key Search on FPGA-Based Parallel Machine "RASH"", Proceedings of Information Processing Society, August 15, 2000, pp. 50-57, Vol. 41, No. SIG5 (HPS1), Japan	<input type="checkbox"/>
	3	DHARMAPURIKAR ET AL., "Design and Implementation of a String Matching System for Network Intrusion Detection using FPGA-based Bloom Filters", Proc. of 12th Annual IEEE Symposium on Field Programmable Custom Computing Machines, 2004, pp. 1-10	<input type="checkbox"/>
	4	KOLONIARI ET AL., "Content-Based Routing of Path Queries in Peer-to-Peer Systems", pp. 1-19, E. Bertino et al. (Eds.): EDBT 2004, LNCS 2992, pp. 29-47, 2004, copyright by Springer-Verlag, Germany	<input type="checkbox"/>
	5	LI ET AL., "Large-Scale IP Traceback in High-Speed Internet: Practical Techniques and Theoretical Foundation", Proceedings of the 2004 IEEE Symposium on Security and Privacy, 2004, pp. 1-15	<input type="checkbox"/>
	6	Office Action for CA Application 2522862 dated May 3, 2010	<input type="checkbox"/>
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	8	Office Action for JP Application 2006-514919 dated August 24, 2010	<input type="checkbox"/>
	9	SEKI ET AL., "High Speed Computation of Shogi With FPGA", Proceedings of 58th Convention Architecture, Software Science, Engineering, March 9, 1999, pp. 1-133-1-134	<input type="checkbox"/>

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	10	YOSHITANI ET AL., "Performance Evaluation of Parallel Volume Rendering Machine Re Volver/C40", Study Report of Information Processing Society, March 5, 1999, pp. 79-84, Vol. 99, No. 21	<input type="checkbox"/>
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